05-04-04

DFS 2823 IFW

Atty. Dkt. No. 039153-0441 (GO406)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Fisher et al.
Title:	ENHANCED TRANSISTOR GATE USING E-BEAM RADIATION
Appl. No.:	10/017,855
Filing Date:	12/14/2001
Examiner:	Julio J. Maldonado
Art Unit:	2823
Confirmation No.:	9701

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: **Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450.**

EV 431586649 US (Express Mail Label Number) 05/03/04 (Date of Deposit)

Roberta A. Cooper (Printed Name)

Roberta A. Cooper (Signature)

TRANSMITTAL OF BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant hereby appeals to the Board of Patent Appeals from the decision of the final rejection dated December 16, 2003, of the Examiner finally rejecting Claims 1-14 and 21-26. The Notice of Appeal was filed on March 3, 2004.

[**X**] Brief on Appeal (20 pages) (in triplicate).

[**X**]To be paid as detailed below

The required fees are calculated below:

[X]	Brief on Appeal Fee	$330.00
[ ]	Extension month:	$0.00
[ ]	Extension:	$0.00
	FEE TOTAL:	$330.00
[ ]	Small Entity Fees Apply (subtract ½ of above):	$0.00
	TOTAL FEE:	$330.00

[X] Check number 13972 in the amount of $330.00 in payment of the Brief on Appeal Fee is enclosed.

[X] The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date 6-3-04

By _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Fisher et al.

Title: ENHANCED TRANSISTOR GATE USING E-BEAM RADIATION

Appl. No.: 10/017,855

Filing Date: 12/14/2001

Examiner: Julio J. Maldonado

Art Unit: 2823

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Roberta A. Cooper (Signature)

BRIEF ON APPEAL

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Under the provisions of 37 C.F.R. § 1.192, this Appeal Brief is being filed in triplicate together with a check in the amount of $330.00 covering the Rule 17(c) appeal fee. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 06-1447.

This paper is being filed in response to the final Office Action dated December 16, 2003 (finally rejecting Claims 1-14 and 21-26). The Notice of Appeal was filed on March 3, 2004. Appellant respectfully requests reconsideration of the application.

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REAL PARTY IN INTEREST

This application has been assigned of record to Advanced Micro Devices, Inc. having a place of business at One AMD Place, 1160 Kern Avenue, Sunnyvale, California 94088-3453. The assignment was recorded in the records of the United States Patent and Trademark Office at Reel/Frame 012389/0709 on December 14, 2001.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

This is an appeal from the final Office Action dated December 16, 2003, finally rejecting Claims 1-14 and 21-26. Claims 15-20 were cancelled without prejudice in a reply dated May 19, 2003 in response to a restriction requirement dated April 24, 2003. Claims 1-14 and 21-26 are therefore on appeal.

STATUS OF AMENDMENTS

No claims have been amended in the present application subsequent to the receipt of the final Office Action dated December 16, 2003.

SUMMARY OF INVENTION

The present invention relates generally to the fabrication of integrated circuits that include transistors (22, 32) having uniform gate widths, reduced gate widths, and preserved minimum extension of the gates onto the field isolation region. (See Specification, page 2, paragraph [0002]).

Currently available lithographic techniques lack the resolution to print sufficiently small IC device features. (See Specification, page 2, paragraph [0004]). For example, present photoresist material used for 193 nm lithography exhibits poor trimming properties (See Specification, page 2, paragraph [0006]).

In one embodiment of the present invention, a polysilicon layer (40) is provided over first and second active regions (24, 34) provided in a substrate (21) on a wafer (20). (See Specification, pages 5-7, paragraphs [0021]-[0025]). A bottom anti-reflective coating (BARC) layer (42) is provided over polysilicon layer (40), after which a layer of photoresist is provided over the BARC layer (42). (See Specification, pages 6-7, paragraphs [0025]-[0026]). The photoresist layer is exposed and developed to define a first gate photoresist feature (26) for a first transistor (22) and a second gate photoresist feature (36) for second transistor (32). (See Specification, page 7, paragraph [0026]).

After developing the photoresist layer, wafer (20) and resist features (6, 36) are exposed to a precisely controlled flood electron beam exposure. (See Specification, page 9, paragraph [0033]). The flood electron beam impinges and penetrates the exposed first and second features (26, 36) and chemically modifies the features to affect their etch characteristics (26, 36). (See Specification, page 9, paragraph [0033]). In particular, a horizontal or trim etch rate, a vertical or erosion etch rate, and an erosion rate of a minimum extension onto isolation regions (30) of each of first and second features (26, 36) are affected to facilitate and control etching of first and second features (26, 36).

E-beam radiation step 12 imparts a chemical change, i.e., cross-linking and decomposition, to the functional groups and additives in the regions of the photoresist material which are bombarded by the electron beam. (See Specification, page 10, paragraph [0037]). Such regions of the photoresist material will accordingly have increased etch resistance (i.e., reduced etch rate), bulk modulus, bulk toughness, and interfacial toughness of the substrate-resist polymer bond (i.e., the bond between the photoresist layer and ARC layer 42). (See Specification, page 10, paragraph [0037]).

After E-beam radiation, wafer 20 is exposed to a plasma etchant to trim or reduce the dimensions of features patterned on the photoresist layer, such as, first and second features (26, 36). (See Specification, page 11, paragraph [0039]). The plasma etchant etches all exposed surfaces between first and second features (26, 36), including the top and side surfaces, to form first and second trimmed gate features (28, 38), respectively (shown in dotted lines in FIGs. 2-4). (See Specification, page 11, paragraph [0040]). Each of first and

second trimmed features (28, 38) has uniformity in width along its length, has maintained a minimum extension onto isolation regions (30), and sufficient thickness or vertical height remains for subsequent transfer of the pattern of features (28, 38) onto underlying layer(s). (See Specification, page 11, paragraph [0041]).

In this manner, transistors having narrow and uniform gate widths can be consistently fabricated. (See Specification, page 12, paragraph [0045]). After the E-beam eradiated gate features have been trimmed, the trimmed gate features enjoy several advantages, including higher uniformity in the gate widths or critical dimensions between gates, higher uniformity in the gate width or critical dimension along the length of a given gate, a narrower gate width, a reduction in consumption of the minimum extension of a given gate onto the field isolation region, and improved control and predictability during the trimming process, than is otherwise possible. (See Specification, page 12, paragraph [0045]).

ISSUES

One issue is presented in this appeal, and is concisely described as follows: whether Claims 1-14 and 21-26 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,139,904 to Auda et al. in view of U.S. Patent No. 6,183,937 to Tsai et al.

GROUPING OF CLAIMS

The grouping of the claims is as follows:

Claims 1-3 and 7 are grouped together as being directed to an integrated circuit fabrication process.

Claim 4 stands alone as being directed to an integrated circuit fabrication process.

Claim 5 stands alone as being directed to an integrated circuit fabrication process.

Claim 6 stands alone as being directed to an integrated circuit fabrication process.

Claims 8 and 12-14 are grouped together as being directed to a method of forming a transistor having a gate width of less than 70 nm.

Claim 9 stands alone as being directed to a method of forming a transistor having a gate width of less than 70 nm.

Claim 10 stands alone as being directed to a method of forming a transistor having a gate width of less than 70 nm.

Claim 11 stands alone as being directed to a method of forming a transistor having a gate width of less than 70 nm.

Claims 21 and 23-26 are grouped together as being directed to a method of producing an integrated circuit.

Claim 22 stands alone as being directed to a method of producing an integrated circuit.

To the extent that the claims in these groups are argued separately below, the claims do not stand or fall together.

ARGUMENT

I. LEGAL STANDARDS

Claims 1-14 and 21-26 have been rejected under 35 U.S.C. § 103(a), which states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The legal standards under 35 U.S.C. § 103(a) are well-settled. Obviousness under 35 U.S.C. § 103(a) involves four factual inquiries: 1) the scope and content of the prior art; 2) the differences between the claims and the prior art; 3) the level of ordinary skill in the pertinent art; and 4) secondary considerations, if any, of nonobviousness. See Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). "'[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 USPQ.2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record."

In re Lee, 277 F.3d 1338, 61 USPQ.2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ.2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

II. REJECTION OF CLAIMS 1-14 AND 21-26 UNDER 35 U.S.C. § 103(a)

In the final Office Action dated December 16, 2003, the Examiner rejected Claims 1-14 and 21-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,139,904 to Auda et al. in view of U.S. Patent No. 6,183,937 to Tsai et al.

Claims 1, 8, and 21 are in independent form. Claims 2-7 depend from Claim 1, Claims 9-14 depend from Claim 8, and Claims 22-26 depend from Claim 21.

For the reasons given below, the Appellant submits that the Examiner's rejection of Claims 1-14 and 21-26 is improper and should be reversed.

A. The Examiner's Rejection of Claims 1-14 and 21-26 Should be Reversed Because There is No Suggestion to Combine the Teachings of Auda et al. with Those of Tsai et al.

To establish a prima facie case of obviousness based on a combination of prior art references under 35 U.S.C. § 103(a), the Examiner must first show that there is a suggestion or motivation to combine the teachings of those references. "There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

On page 5 of the final Office Action dated December 16, 2003, the Examiner provided the following asserted motivation to combine the teachings of Auda et al. and Tsai et al. (with emphasis added):

> [T]he teachings of Auda et al. and Tsai et al. are directed to the formation of fine patterns either by trim etching (as taught by Auda et al.) or by photoresist decomposition (as taught by Tsai et al.). As established in the prior office action, by including the curing process of Tsai et al. prior to the trim etching of Auda et al. would result in a patterned photoresist layer having a narrower linewidth as taught by Tsai et al., resulting in an even narrow line width pattern in Auda et al. Therefore, there is motivation to combine their teachings and a prima facie case of obviousness exists.

The cited references, as noted by the Examiner, relate to two entirely separate and distinct ways of forming "fine patterns." There is no teaching or suggestion in either of these references that would have motivated one of ordinary skill in the art to combine their teachings in the manner suggested by the Examiner. For example, Tsai et al. does not indicate that the "linewidth dimension" of the features could be further reduced by using "reactive ion etching" such as that used in Auda et al. Nor is there any teaching or suggestion in either of the references that such a combination would even be possible. For example, there is no discussion of how process parameters may have to be modified in order to perform each of the methods disclosed in Auda et al. and Tsai et al.

Instead of identifying a specific objective motivation to combine the teachings of Auda et al. and Tsai et al., the Examiner has instead speculated that taking elements from two otherwise unrelated references and combining them would result in the combination of elements recited in the claims of the present application. However, such reasoning constitutes improper hindsight reconstruction of the Appellants' claimed invention, and the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ.2d 1430 (Fed. Cir. 1990).

It is insufficient that the modification of Auda et al. and Tsai et al. asserted by the Examiner may have been within the capabilities of one of ordinary skill in the art at the time

of the invention, without a separate motivation to make the combination. As noted by the Board of Patent Appeals and Interferences, a statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

The rejection of Claims 1-14 and 21-26 should be reversed, because there is no suggestion or motivation to combine the teachings of Auda et al. with those of Tsai et al. to obtain the subject matter recited in these claims.

B. The Examiner's Rejection of Claims 1-14 and 21-26 Should be Reversed Because the Combination of Auda et al. and Tsai et al. Does Not Teach or Suggest At Least One Element of Each of the Rejected Claims

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Even if Auda et al. and Tsai et al. could be properly combined, these references do not teach or suggest at least one element of each of Claims 1-14 and 21-26. Accordingly, the rejection of these claims under 35 U.S.C. § 103(a) is improper and should be reversed.

Independent Claim 1 recites an "integrated circuit fabrication process," including, among other limitations, "curing the transistor gate pattern with an electron beam" and "trimming the cured transistor gate pattern" (emphasis added).

Independent Claim 8 recites a "method of forming a transistor having a gate width of less than 70 nm," including, among other limitations, "E-beam irradiating a gate pattern of a photoresist layer" and "trimming the E-beam irradiated gate pattern of the photoresist layer" (emphasis added).

Independent Claim 21 recites a "method of producing an integrated circuit," including, among other limitations, "irradiating a portion of the photoresist material with an electron beam to form a gate pattern" and "trimming the gate pattern" (emphasis added).

One nonexclusive example of a trimming operation is described in paragraphs [0039] and [0040] of the present application:

> After E-beam radiation step 12, wafer 20 undergoes resist trimming step 14. Trimming step 14 is preferably a plasma etching step. Wafer 20 is exposed to a plasma etchant to trim or reduce the dimensions of features patterned on the photoresist layer, such as, first and second features 26, 36. The plasma etchant can comprise a variety of plasma etch chemistries, such as, O_2, HBr/O_2, Cl_2/O_2, $N_2/He/O_2$, or N_2/O_2. A variety of standard etching equipment, such as those manufactured by Applied Materials of Santa Clara, California, or Lam Research of Freemont, California, may be utilized to provide the plasma etchant. An exemplary trim/gate stack etch can employ HBr/O2/Ar chemistry for the resist trim, CF4/Ar chemistry for the ARC etch, and a sequence of steps employing one or more of HBr, HeO2, CF3, and CI2 for the poly silicon etch.
>
> The plasma etchant etches all exposed surfaces between first and second features 26, 36, including the top and side surfaces, to form first and second trimmed gate features 28, 38, respectively (shown in dotted lines in FIGs. 2-4). Because different regions or portions of each of first and second features 26, 36 have different etch rates relative to each other following E-beam radiation step 12 (e.g., vertical etch rate vs. horizontal etch rate), the dimensional reduction of all of the surfaces of first and second features 26, 36 is not the same.

There is no teaching or suggestion in either of Auda et al. or Tsai et al., alone or in proper combination, to "trim" a gate pattern that had previously been "cured" (Claim 1) or "irradiated" (Claims 8 and 21).

For example, as noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." Auda et al. relates to a "method of producing high resolution and reproducible patterns" and discloses that a "film 17 of a standard photoresist material" is "imaged with UV radiation" to form a "photoresist pattern 17a" that is "placed in reactive ion etching (RIE) equipment and the resist pattern is isotropically eroded to reduce overall dimensions" (Abstract; Column 5, lines 30-63) (emphasis added). There is no

teaching or suggestion in Auda et al. that the "photoresist pattern 17a" has been cured or irradiated prior to placement in the reactive ion etching equipment and subsequent etching.

Tsai et al. also does not teach or suggest trimming a photoresist pattern that has been cured (Claim 1) or irradiated (Claims 8 and 21) with an electron beam. Tsai et al. relates to a "post photodevelopment isotropic radiation treatment method for forming patterned photoresist layer with attenuated linewidth" and discloses the use of a "photoresist material which is susceptible to radiation induced conformal surface layer decomposition and attendant shrinkage" (Column 6, lines 3-6) (emphasis added). Thus, instead of trimming a photoresist pattern that has been cured (Claim 1) or irradiated (Claims 8 and 21), Tsai et al. discloses the use of a material that shrinks upon exposure to radiation. There is no teaching or suggestion in Tsai et al. to trim such any material that has previously been cured or irradiated.

The Examiner stated in the final Office Action dated December 16, 2003 that "by using the curing process of Tsai et al. in the patterning process of Auda et al., one of ordinary skill in the art would arrive to the claimed invention." However, the Examiner's argument assumes that there is some teaching or suggestion in the references that the reactive ion etching described in Auda et al. could be used with the material used in Tsai et al. that undergoes "radiation induced conformal surface layer decomposition." Neither of these references, alone or in combination, can be said to properly teach or suggest such a result. Because the teaching or suggestion to trim a previously cured or irradiated gate pattern comes only from the Appelants' own disclosure, the rejection of Claims 1, 8, and 21 (and their associated dependent claims) is improper and should be reversed.

The rejection of Claims 1-14 and 21-26 should be reversed, because at least one limitation of independent Claims 1, 8, and 21 is not taught or suggested by the combination of Auda et al. and Tsai et al.

C. The Examiner's Rejection of Claims 5 and 9 Should be Reversed Because the Combination of Auda et al. and Tsai et al. Does Not Teach or Suggest At Least One Element of the Rejected Claims

Even if Auda et al. and Tsai et al. could be properly combined, these references do not teach or suggest at least one element of each of Claims 5 and 9. Accordingly, the rejection of these claims under 35 U.S.C. § 103(a) is improper and should be reversed.

Claim 5 recites "wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100000 $\mu C/cm^2$." Claim 9 recites "wherein the E-beam irradiating step uses an electron beam at a dose in the range of approximately 100-100000 $\mu C/cm^2$."

As noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." While Tsai et al. discloses that "the types of radiation employed . . . include . . . electron radiation" (Column 6, lines 26-34), there is no teaching or suggestion as to the dosages recited in Claims 5 and 9.

The Appellants have identified a particular range for the electron beam dose that is not taught or suggested by the combination of Auda et al. and Tsai et al. Such dose is selected to provide optimum desirable etch trimmability and etch stability characteristics during resist trimming, and may vary depending on the type of photoresist material, subsequent processing steps involving the E-beam eradiated photoresist, and/or desired characteristics of the photoresist material (See, e.g., Specification, page 9, paragraph [0035]).

The ranges for the electron beam doses are taught only by Appellants' own disclosure. Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claims 5 and 9, and therefore the rejection of Claims 5 and 9 should be reversed.

D. The Examiner's Rejection of Claim 6, 10, and 22 Should be Reversed Because the Combination of Auda et al. and Tsai et al. Does Not Teach or Suggest At Least One Element of Each of the Rejected Claims

Even if Auda et al. and Tsai et al. could be properly combined, these references do not teach or suggest at least one element of each of Claims 6, 10, and 22. Accordingly, the rejection of these claims under 35 U.S.C. § 103(a) is improper and should be reversed.

Claim 6 recites "wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 50-2000 Volts." Claim 10 recites "wherein the electron beam is provided at an accelerating voltage in the range of approximately 50-2000 Volts." Claim 22 recites "wherein the electron beam is provided at an accelerating voltage in the range of approximately 0.5-50 Kv."

As noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." While Tsai et al. discloses that "the types of radiation employed . . . include . . . electron radiation" (Column 6, lines 26-34), there is no teaching or suggestion as to the voltage ranges recited in Claims 6, 10, and 22.

The Appellants have identified a particular range for the accelerating voltage that is not taught or suggested by the combination of Auda et al. and Tsai et al. Such voltage is selected to provide optimum desirable etch trimmability and etch stability characteristics during resist trimming, and may vary depending on the type of photoresist material, subsequent processing steps involving the E-beam eradiated photoresist, and/or desired characteristics of the photoresist material (See, e.g., Specification, page 9, paragraph [0035]).

The ranges for the electron beam accelerating voltages are taught only by Appellants' own disclosure. Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claims 6, 10, and 22, and therefore the rejection of Claims 6, 10, and 22 should be reversed.

E. The Examiner's Rejection of Claims 4, 8, and 21 Should be Reversed Because the Combination of Auda et al. and Tsai et al. Does Not Teach or Suggest At Least One Element of Each of the Rejected Claims

Claim 4 recites "wherein the final gate transistor width is in the range of approximately 20-60 nm." Claim 8 recites "the gate width being less than 70 nm." Claim 21 recites "the gate having a width of less than 70 nm."

There is no teaching or suggestion in either Auda et al. or Tsai et al. that gate widths such as those recited in Claims 4, 8, or 21 may be achieved using the methods recited in Auda et al. or Tsai et al., either alone or in any proper combination.

For example, Auda et al. states that "the method of the present invention allows production of polysilicon line widths of 600 nm with a precision of +/- 180 nm" (Column 10, lines 48-49). Tsai et al. discloses "patterned phororesist line linewidths" of between approximately 188 and 230 nm (Column 12, Table I).

The subject matter of the claims of the present application allow for the consistent formation of transistors having narrow and uniform gate widths (See, e.g., Specification, page 12, paragraph [0045]). Neither Auda et al. nor Tsai et al. contemplate the formation of gates having such dimensions, and therefore the subject matter recited in Claims 4, 8, and 21 would not have been obvious to one of ordinary skill in the art at the time of the invention.

Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claims 4, 8, and 21, and therefore the rejection of Claims 4, 8, and 21 should be reversed.

F. The Examiner's Rejection of Claim 11 Should be Reversed Because the Combination of Auda et al. and Tsai et al. Does Not Teach or Suggest At Least One Element of Each of Claim 11

Claim 11 recites "wherein a uniformity of the gate width is 4 to 6 nm over a 3 nm segment." Auda et al. and Tsai et al., alone or in proper combination, do not teach or suggest the subject matter recited in Claim 11. The Examiner stated:

> The combined teachings of Auda et al. and Tsai et al. substantially teach all aspects of the invention but fail to show . . . wherein the uniformity of the gate width is 4 to 6 nm over a 3 nm segment. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension.

In contrast to the Examiner's suggestion, producing a gate having a width that has uniformity of 4 to 6 nm over a 3 nm segment would not have been an "obvious matter of design choice." As noted in the present application (with emphasis added):

> For example, transistor gates patterned using 193 nm lithography and a typical commercially available photoresist material can have critical dimensions (CDs) of 130-110 nm before the resist trimming process and the final critical dimensions (CDs) of approximately 70-80 nm after the resist trimming process. Any further trimming would typically result in non-uniform widths along the length of the gates, unacceptable consumption of the minimum extension of the gates onto the field isolation regions, (i.e. unacceptably large end of the line pull back) and/or excessive thinning of the gate pattern over topography steps such that pattern transfer to the underlying layer(s) of the wafer is not possible. Such poor trimming results can affect the operating conditions and/or performance of the transistors to the extent that the resist trimming process will become unusable without violating design rules for given technology scaling requirements.
>
> Preferably, first and second gates 70, 74 have gate widths comparable to width 60. First gate 70 includes a minimum extension 72 onto isolation regions 30 and second gate 74 includes a minimum extension 76 onto isolation regions 30. Each of minimum extensions 72, 76 has a length comparable to extended length 62. The width along the length of each of first and second gates 70, 74 has a variation of less than 1 nm, as opposed to a gate formed from photoresist that was not e-beam eradiated which has a gate width variation along its length of approximately 5 nm. In one embodiment, the local gate width variation is between 4 to 6 nm over a 3 nm gate length (3 sigma). Preferably this variation can be further reduced as technology permits.

Thus, as noted in the present application, the dimensions recited in Claim 11 are not merely a matter of "routine experimentation and optimization" as indicated by the Examiner, but rather represent a non-obvious advance over previous attempts at controlling gate width variations.

Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claim 11, and therefore the rejection of Claim 11 should be reversed.

CONCLUSION

In view of the foregoing, the Appellant submits that Claims 1-14 and 21-26 are not properly rejected under 35 U.S.C. § 103(a) over the combination of Auda et al. and Tsai et al. and are patentable.

Accordingly, Appellant respectfully requests that the Board reverse all claim rejections and indicate that a Notice of Allowance respecting all pending claims should be issued.

Respectfully submitted,

Date 5-3-04

By _____

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APPENDIX - THE CLAIMS ON APPEAL

1. An integrated circuit fabrication process, the process comprising the steps of:

patterning a transistor gate pattern on a photoresist layer;

curing the transistor gate pattern with an electron beam;

trimming the cured transistor gate pattern; and

transferring the trimmed transistor gate pattern to a layer disposed below the trimmed pattern to form a transistor gate, wherein the transistor gate includes a width and a length, and a variation of the width along the length of the transistor gate is reduced due to the curing step.

2. The process of claim 1, wherein the photoresist layer is comprised of a photoresist material used for at least one of 248 nm lithography, 193 nm lithography, and extreme ultraviolet light (EUV) lithography.

3. The process of claim 2, wherein the photoresist layer is comprised of a photoresist material of a type used for 193 nm and 248 nm lithography and is commercially available.

4. The process of claim 1, wherein the final gate transistor width is in the range of approximately 20-60 nm.

5. The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100000 $\mu C/cm^2$.

6. The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 50-2000 Volts.

7. The process of claim 1, wherein the curing step includes changing at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the transistor gate pattern.

8. A method of forming a transistor having a gate width of less than 70 nm, the method comprising the steps of:

E-beam irradiating a gate pattern of a photoresist layer;

trimming the E-beam irradiated gate pattern of the photoresist layer; and

etching a polysilicon layer disposed below the photoresist layer in accordance with the trimmed gate pattern to form a gate of the transistor, the gate width being less than 70 nm.

9. The method of claim 8, wherein the E-beam irradiating step uses an electron beam at a dose in the range of approximately 100-100000 $\mu C/cm^2$.

10. The method of claim 9, wherein the electron beam is provided at an accelerating voltage in the range of approximately 50-2000 Volts.

11. The method of claim 9, wherein a uniformity of the gate width is 4 to 6 nm over a 3 nm segment.

12. The method of claim 9, wherein the photoresist layer is comprised of a material selected from a group consisting of an acrylate-based polymer, alicyclic-based polymer, phenolic-based polymer, and a polystyrene-based polymer.

13. The method of claim 9, wherein the E-beam irradiation step includes affecting at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the gate pattern of the photoresist layer.

14. The method of claim 9, wherein the E-beam radiation step achieves an enhancement interim rate for a commercially available resists using lithography processes with either 248 nm and 193 nm wavelength of light.

21. A method of producing an integrated circuit comprising:

providing a photoresist material over a substrate;

irradiating a portion of the photoresist material with an electron beam to form a gate pattern;

trimming the gate pattern; and

etching the substrate in accordance with the gate pattern to form a gate, the gate having a width of less than 70 nm.

22. The method of claim 21, wherein the electron beam is provided at an accelerating voltage in the range of approximately 0.5-50 Kv.

23. The method of claim 21, wherein the photoresist layer is comprised of a material selected from a group consisting of an acrylate-based polymer, an alicyclic-based polymer, a phenolic-based polymer, and a polystyrene-based polymer.

24. The method of claim 21, wherein the step of irradiating a portion of the photoresist material includes affecting at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the gate pattern of the photoresist layer.

25. The method of claim 21, wherein the step of irradiating a portion of the photoresist material achieves an enhancement interim rate for a photoresist material using lithography processes with either 248 nm and 193 nm wavelength of light.

26. The method of claim 21, wherein the photoresist material may be used with at least one of 248 nm lithography, 193 nm lithography, and extreme ultraviolet (EUV) lithography.